Remarks

The final Office Action dated November 5, 2004, indicated that claims 18 and 19 are allowed. After the above cancellation of claims 1-9, the remaining rejections are as follows: claims 15-17, 24, and 26 stand rejected under 35 U.S.C. § 102(b) in view of of *Asai et al.* (U.S. Patent 5,553,309); and claims 10-14, 20, and 21 stand rejected under 35 U.S.C. § 102(b) in view of *Inagami et al.* (U.S. Patent No. 4,881,168). Applicant respectfully traverses the rejections because they are not based on a consistent and proper interpretation of the claims and because they ignore important claim terms. For example, claim terms "computation" and "arithmetic cluster" appear to have been ignored altogether. Such deficiencies are addressed for each rejection in the following discussion which provides examples of the noncorrespondence between the claim limitations and the teaching of the asserted references.

Regarding the rejection of claims 10-14 and 20, the '168 reference does not teach or suggest the claimed "arithmetic cluster". The '168 reference does not correspond to provide any assertion for correspondence to this claim term. Thus, the claimed limitation(s) do not correspond and each claim when considered as a whole is not invalid under §102(b). For related use of this claim term and related terms in the Specification, reference may be made to page 11, lines 15-20, and FIG. 2.

Applicant submits that the rejection of claims 10, 11 and 14 should also fail because claim limitations have been ignored or misconstrued. For example, the '168 reference does not teach or suggest the claimed "length of the condition vector being greater than a length of the input vector". Applicant appreciates Examiner's clarifications on page 4 items 10 and 11 alleging the length of the input buffer; however, Applicant respectfully disagrees with Examiner's assessment that "the input buffer consists of ten elements, A0-A9" because Figure 4, element 21, of the '168 reference clearly shows sixteen elements A0-A15, the same number of elements as the mask vector 22. Thus, the '168 reference teaches that the mask vector and input buffer have equal lengths, which does not correspond to the claimed "length of the condition vector being greater than a length of the input vector."

With regards to the rejection of claims 15-17, Applicant submits that this rejection must fail because the '309 reference does not teach or suggest the claimed "computation" as used, for example, in the claim term "each output element is a result of a computation

performed on each corresponding intermediate element". The '309 reference teaches storing of an output element in a memory without any such computation involved, and the Office Action does not cite any evidence in support of corresponding teaching for this aspect of the claimed invention. Therefore, the claimed limitation(s) do not correspond and each claim when considered as a whole is not invalid under §102(b).

With regards to the rejection of claim 21, Applicant submits that this rejection should also fail because the limitations concerning the claimed iteration do not correspond to the iteration discussed in the '168 reference. On page 5 item 13, the Office Action states the '168 reference "have taught an iteration, see column 7, lines 8-14". At column 7, lines 8-14, the '168 reference teaches repeated steps to sequentially store elements of vector data, with each element stored exactly once. In contrast, claim 21 concerns iterations that are directed to processing the same element multiple times. Thus, the repeated steps taught in the '168 reference do not correspond to the claimed iterative processing of the input vector.

Applicant submits that the rejection of claim 24 fails because its claim limitations have been interpreted inconsistently, for example, in connection with the claimed "plural clusters" which are not taught by the '309 reference. On page 3 item 7, the Office Action attempts to support the rejection as follows: "in Figure 6, component A(1) is a processing cluster that generates an output vector element A(1) in output vector register 2, component A(4) is a processing cluster that generates an output vector element A(4) in output vector register 2, and component A(5) is a processing cluster that generates an output vector element A(5) in output vector register 2, etc." Applicant respectfully disagrees with Examiner's assessment that each A(1), A(4), and A(5), *etc.* should be construed on one hand to be a "processing cluster" and on the other hand as data values per "an output vector element." Clearly, A(1), A(4), and A(5), etc. are values of an array A() with respective element indices 1, 4, and 5, *etc.* and they do not form a cluster. Accordingly, Applicant respectfully traverses the rejection.

Applicant submits that the rejection of claim 26 fails because a number of limitations have also been ignored or misconstrued. On page 4 item 9 of the Office Action, Examiner states: Applicant has not claimed a device that configures a switch "so that the switch is capable of transferring the input and output vector elements between any of the first plurality of entries of the buffer" and as such this limitation is not read into the claims.

Applicant respectfully submits that the Examiner is mistaken because claim 26 reads in part (italics added):

> *a controller* to direct conditional vector input and output operations by controlling reading the input and the output vector elements from the buffer, by controlling receiving the input and the output vector elements into the buffer; by processing the condition vector elements, and by *configuring the switch so that the switch is capable of transferring the input and output vector elements between any of the first plurality of entries of the buffer*, any of the second plurality of entries of the buffer, and any of the plurality of processing elements.

Accordingly, Applicant respectfully disagrees with Examiner's characterization in item 9 on page 4 of the Office Action that "this argument is moot". Further, the '309 reference teaches a data selection circuit limited to receiving elements from an input vector register and sending elements to a compress circuit. The '309 reference does not teach nor suggest a switch capable of the claimed "transferring the input and output vector elements between any of the first plurality of entries of the buffer, any of the second plurality of entries of the buffer, and any of the plurality of processing elements".

In view of the above discussion, Applicant believes that the rejection has been overcome and the application is in condition for allowance. A favorable response is requested. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is encouraged to contact the undersigned at (651) 686-6633.

Respectfully submitted,

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